IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Gopakumar Parameswaran, Cuong C. Ly, Douglas L. Yanagawa, Mark N. Yamashita and Yuval Bachar
Assignee:	Cisco Technology, Inc.
Title:	SYSTEM AND METHOD FOR REDUCING CROSSTALK BETWEEN VIAS IN A PRINTED CIRCUIT BOARD

Application No.:	10/727,381	Filing Date:	December 4, 2003
Confirmation No.:	7407	Date Allowed:	March 28, 2007
Examiner:	Jeremy C. Norris	Group Art Unit:	2841
Docket No.:	CIS0203US		

Austin, Texas
March 27, 2007

Attention: Official Draftsperson
Mail Stop Issue Fee
COMMISSIONER FOR PATENTS
P. O. Box 1450
Alexandria, VA 22313-1450

SUBMISSION OF FORMAL DRAWINGS

Dear Sir:

Applicants submit five (5) sheets of formal drawings, consisting of Figures *1, 2A & 2B, 3, 4 & 5 and 6* in the above-named application. If there are any questions regarding these drawings, please call the undersigned at (512) 439-5080.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to Attention: Official Draftsperson, Mail Stop Issue Fee, Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on March 27, 2007.

Brenna A Brock — Attorney for Applicant(s)

3-27-2007 — Date of Signature

Respectfully submitted,

Brenna A Brock

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